Computer Modeling of Dielectric Relaxation in Semi-Insulating Materials and Devices for Electrophotography

Ming-Kai Tse*, Inan Chen, and David J. Forrest

Quality Engineering Associates (QEA), Inc., Burlington, MA, USA

The physics of dielectric relaxation in semi-insulating materials is critical to the performance of devices such as the rollers and belts used in electrophotography. In recent years we have investigated the basic principles of dielectric relaxation and a practical method of device characterization called Electrostatic Charge Decay (ECD). We have also developed computer models to simulate dielectric relaxation in semi-insulators in EP subsystems from first principles of charge transport theory. In this paper, we describe our computer modeling methodology and its applications to the simulation of EP subsystems and the ECD method. Examples from the numerical analysis are shown, together with ECD measurement results, to demonstrate the non-Ohmic nature and the critical role of charge injection in dielectric relaxation.

1. Introduction

In electrophotography (EP), devices such as rollers and belts are used in toner development and transfer, as well as in charging photoreceptors. The structure of these devices consists of a thin semi-insulating (SI) dielectric layer on a conductive substrate (or shaft). The SI dielectric layer comes in contact with an insulator layer (toner and/or photoreceptor). A bias voltage is applied across the two layers, as shown schematically in Fig.1. It has been shown that efficient decay of the voltage across the SI dielectric layer (i.e., dielectric relaxation) is important for efficient performance of the sub-processes.[1-4]

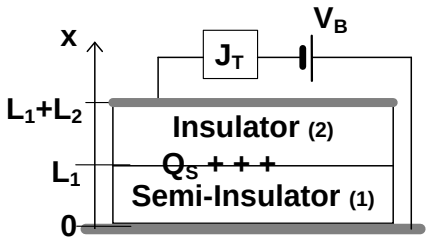

Fig.1. Series-capacitor model of rollers/belts in EP sub-processes.

To analyze the dielectric relaxation in SI, a simple RC equivalent circuit model is often applied. In this model, the voltage across the dielectric layer is expected to decay exponentially (dielectric relaxation) with a time constant $\tau = RC$, where R is the resistance of the dielectric layer and C is the sum of the capacitances of the two layers.[4] In this model, a key controlling variable for dielectric relaxation is the resistance R in the semi-insulator, and the prevailing technique for evaluating semi-insulating devices is to measure the resistance.

The traditional electrical resistance measurement method involves applying a DC voltage V between an electrode on the roller/belt surface and the conductive substrate/shaft. The resulting current I (or current density $J = I/A$, where A = electrode contact area) is measured, and the roller/belt resistance is computed using Ohm's law, $R = V/I$ or V/J. While this traditional approach is straightforward in principle, the relevance of the results for predicting EP device performance is questionable for a number of reasons:

1) Resistance $R = L/\sigma$, where L is the layer thickness and σ the conductivity. The latter is the product of mobility μ, and the intrinsic charge density q_i, $\sigma = \mu q_i$. In semi-insulating devices, it has been shown[2] that μ and q_i influence the dielectric relaxation process independently and hence, not surprisingly, measurement of R or σ alone cannot predict EP device performance reliably.
2) Both R and σ are bulk properties independent of the contact condition at the interface with the electrodes. The measured current is determined by the resistance only if the electrode can supply charges sufficiently to maintain the intrinsic value q_i (i.e., Ohmic contact). However, in most EP rollers/belts, the contact between the SI dielectric layer and the substrate is non-Ohmic in nature. The charge injection from the contact depends on the amount of free charge available and the field strengths at the contact, and on the mechanical conditions (e.g. pressure, adhesion, smoothness) of the interface.
3) Intrinsic charge density q_i is typically very low in semi-insulators. Consequently, the steady state current measured in the resistance measurement method is unlikely governed by the intrinsic charge,

Quality Engineering Associates (QEA), Inc.
99 South Bedford Street, #4, Burlington, MA, USA 01803
Tel. 1-781-221-0080, Fax. 1-781-221-7107
Email: mingkaitse@att.net, mingkaitse@qea.com

but rather, controlled by the injected charge from the interface. In other words, the traditional resistance method does not really measure the bulk resistance (or conductivity) as assumed in the Ohmic model.

4) In resistance measurement, a constant voltage is applied across the semi-insulator; whereas in an EP sub-system (Fig. 1), the bias voltage is applied not only to the SI dielectric layer, but also to layers of insulators (photoreceptor, toner layer and/or air-gap) in series. As such, the voltage across the SI layer is not constant but decreases with time. This causes the field, and hence the charge injection from the substrate, to vary with time. In other words, the rollers/belt in EP sub-processes is in an open-circuit condition, not the closed-circuit condition applied in resistance measurement.
5) Real-world EP devices are likely to exhibit some degree of non-uniformity. Another disadvantage of the resistance contact measurement method is that it does not lend itself to mapping of the entire device.

To circumvent the shortcomings of the traditional resistance measurement method and to enable efficient, non-destructive mapping of rollers and belts, we have introduced an EP device characterization technique called "Electrostatic Charge Decay" (ECD).[5-7] In the ECD method, the test sample on a grounded substrate is charged with a scanning corona at the surface. During scanning, the current through the sample to ground and the surface voltage are measured, the latter by means of a non-contact electrostatic probe immediately following the charger. A schematic of the ECD method is shown in Fig. 2. In the voltage mode, the decay of surface voltage at a position is monitored after the charging corona passes that position. In the current modes, the decay of corona current with charging time (and with the build-up of surface voltage) is monitored. The time and space dependent voltage or current provide quantification of the dielectric relaxation in the SI. Because of the use of a scanning corona and non-contact voltage probe, the technique enables non-destructive, efficient mapping of a large area of the sample for evaluation of device uniformity.

2. Computer Simulation - Series Capacitor Model of EP Subsystems and the ECD Method

With the charge mobility μ in a typical semi-insulator used in electrophotography as low as 10^{-5}cm^2/V-sec, the transit time required for a charge to move across a layer of thickness $L \approx 100$ μm in a field $E \approx 10^5$ V/cm is $t_T = L/\mu E \approx 10^{-2}$ sec. This is the same order of magnitude (if not longer) as the dielectric relaxation time computed from permittivity and conductivity, i.e., $t_R = \varepsilon/\sigma \approx 10^{-3}$ sec, with permittivity $\varepsilon \approx 10^{-13}$ F/cm and conductivity $\sigma \approx 10^{-10}$ S/cm. Under this condition of $t_T \approx > t_R$, space charge effects, i.e., the influence on the motion of a charge from other charges, cannot be ignored in the relaxation process.

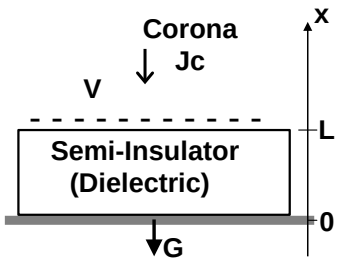

Fig.2. Schematic of an ECD test.

The motion of charges in the SI layer is described by the continuity equation for the positive (or negative) charge densities q_p (or q_n). Omitting subscripts p and n,

$$\partial q(x, t)/\partial t = -\partial J/\partial x = -(\partial/\partial x)(\mu q E) \quad (1)$$

where $J(x, t) = \mu q E$ is the conduction current density, μ is the charge mobility and $E(x, t)$ is the electric field in the SI layer. The boundary condition at the substrate interface, $x = 0$ in Figs.1 and 2, is specified by the current injected into the dielectric layer, $J(0, t)$. This injection can be expected to increase with the field $E(0, t)$ at the interface. For lack of more precise knowledge, it is sufficient to assume that it is linearly proportional to $E(0, t)$, with a proportionality constant s specifying the injection strength:

$$J_p(0, t) = sE(0, t), \text{ and } J_n(0, t) = 0, \text{ if } E(0, t) > 0 \quad (2a)$$

$$J_p(0, t) = 0, \text{ and } J_n(0, t) = sE(0, t), \text{ if } E(0, t) < 0 \quad (2b)$$

In the series-capacitor configuration (Fig.1), there is no conduction current and no charge injection into the insulator from the top electrode at $x = L_1 + L_2$. Another boundary condition relates the charge $Q_S(t)$ accumulated at the interface ($x = L_1$) to the fields in the two layers at the interface $x = L_1$ by Gauss' Theorem as,

$$Q_S(t) = \varepsilon_2 E_2(t) - \varepsilon_1 E_1(L_1, t) \quad (3)$$

where ε_1 and ε_2 are the permittivity of the SI layer and insulator layer, respectively. The field $E_1(x, t)$ in the SI layer is related to the charge densities by Poisson's equation,

$$\partial E_1(x, t)/\partial x = [q_p(x, t) + q_n(x, t)]/\varepsilon_1 \quad (4)$$

In the insulator, the bulk charge density is always zero, and hence, the field $E_2(t)$ is always uniform in x.

At $t = 0$, the bulk charge densities have the intrinsic values, $q_p(x, 0) = -q_n(x, 0) = q_i$, and the interface charge is $Q_S(0) = 0$. Noting that $E_1(x, 0)$ is also uniform in x, Eq.(3) gives the initial fields and voltage divisions as,

$$V_1(0) = -E_1(x, 0)L_1 = -V_B L_1/\varepsilon_1(L_1/\varepsilon_1 + L_2/\varepsilon_2) \quad (5a)$$

$$V_2(0) = -E_2(0)L_2 = -V_B L_2/\varepsilon_2(L_1/\varepsilon_1 + L_2/\varepsilon_2) \quad (5b)$$

where the applied bias voltage is $V_B = V_1(0) + V_2(0)$.

In the ECD experiments (Fig.2), the corona current, $J_C(t)$, incident on the SI surface can be represented by,

$$J_C(t) = J_{mx}[1 - V(t)/V_{mx}] \quad (6)$$

where J_{mx} and V_{mx} are empirically determined parameters, representing the initial (maximum) current and the final (maximum) voltage, respectively. The surface charge density $Q_S(t)$ varies with time as J_C deposits charges on the surface, and the positive and negative conduction currents J_p and J_n in the layer arrive at the surface:

$$dQ_S/dt = -J_C(t) + J_p(L, t) + J_n(L, t) \quad (7)$$

The field at the surface $x = L$ is related to Q_S by Gauss' theorem: $\varepsilon E(L, t) = -Q_S(t)$, where ε is the sample permittivity. The injection of (corona) charge from the surface into the SI layer is practically negligible. Starting from the initial conditions that $Q_S(0) = 0$, $V(0) = 0$, $E(x, 0) = 0$, $q_p(x, 0) = -q_n(x, 0) = q_i$, and $J_C(0) = J_{mx}$, the build-up of the layer voltage $V(t)$ and the decay of corona current $J_C(t)$ can be calculated from the continuity equation, Eq.(1), and the injection currents, Eq.(2). The decay of surface voltage after the termination of corona charging can be examined by setting $J_C = 0$ in the above procedure.

To examine the progress of dielectric relaxation of the SI layer, the voltage and/or the current are calculated by numerical iterative solution of the above equations. The computation procedure is illustrated in the flow chart shown in Fig.3.

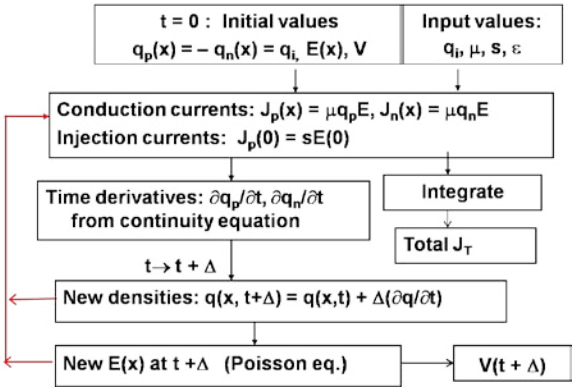

Fig.3. Flow chart of numerical procedure for modeling dielectric relaxation.

3. Examples of Numerical Simulation of Dielectric Relaxation

In the following discussion and figures, the normalized units in voltage, current and time are defined in Table 1.

An example of numerical results for the dielectric relaxation in the series-capacitor configuration (Fig.1) is shown in Fig.4. The thickness L_2 and the permittivity ε_2 of the insulator are assumed (without loss of generality) to be ½ of the corresponding values of the SI layer. Thus, both layers have the same capacitance $C = \varepsilon/L$, and the same initial voltage $V_1(0) = V_2(0) = V_B/2$. The strength of charge injection from the substrate s is varied over more than 3 orders of magnitude, while the intrinsic charge density is assumed to have a small value $q_i = 0.1$.

Table 1. Normalized units used in the figures

Unit	Definition	Typical value
Thickness L_0	SI thickness	10^{-2} cm
Voltage V_0	Bias voltage	10^{3} V
Permittivity ε_0	SI's	3×10^{-13} F/cm
Mobility μ_0	Hole's in SI	10^{-5} cm^2/Vsec
Time t_0	$= L_0^2/\mu_0 V_0$	10^{-2} sec
Charge density q_0	$= \varepsilon_0 V_0/L_0^2$	3×10^{-6} Coul/cm^3
Current density J_0	$= \varepsilon_0\mu_0 V_0^2/L_0^3$	3×10^{-6} Amp/cm^2
Injection strength s_0	$= \mu_0 q_0$	3×10^{-11} S/cm

An important observation in Fig.4 is that voltage relaxation in semi-insulator is non-ohmic, i.e., not exponential or, nonlinear in a plot of V vs log time t as predicted by an RC model. Instead, the relaxation is controlled mostly by the injection strength s at the low charge density level analyzed. On the other hand, at high charge density (for $q_i \geq 1$), similar calculations show that relaxation is almost independent of injection s.

In Fig.4, the time required for full decay increases as s decreases ($\approx 1/s$). Such dependence of relaxation characteristics on charge injection is not considered by the simple RC equivalent circuit model.

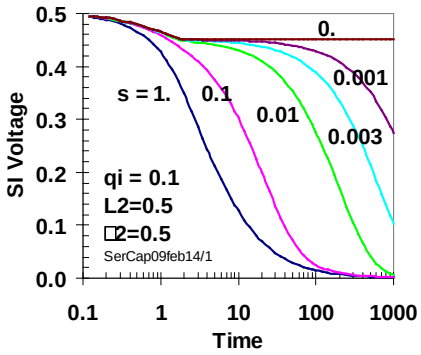

Fig.4. Decay of SI layer voltage with time, for various values of charge injection strength s.

Fig.5 shows the numerical results of decay of charging currents (solid curves) and the rise of surface voltage (dashed curves) with time during an ECD test of a semi-insulating sample (Fig. 2). After a charging time $t \geq 100$, both the current and the voltage reach steady state values which are dependent on the injection strength s. On the other hand, similar simulations using q_i and μ in a broad range of practical interest show that the steady state voltage and current values are practically independent of these parameters. Utilizing such knowledge obtained through numerical analysis, the steady state current measured by the ECD method in the current mode (Fig.6) can be used to estimate the injection strength s.[6]

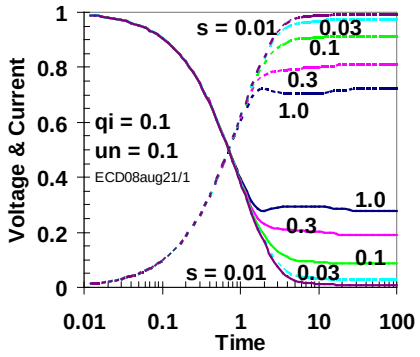

Fig. 5. Decay of charging current (solid curves) and rise of surface voltage (dashed curves) with time in ECD experiments for various injection strength *s*.